**MINI PROJECT**

**Controller Area Network Transmission Module Using Verilog HDL**

**TESTBENCH CODE:**

module can\_tx\_tb;

parameter CLK\_PERIOD = 10;

parameter SIM\_TIME = 500;

// Signals

reg clk = 0;

reg baud\_clk = 0;

reg rst = 1;

reg send\_data = 0;

reg bitstuffed\_output = 0;

reg clear\_to\_tx = 1;

reg rx = 0;

reg [10:0] address = 11'd0;

reg [7:0] data = 8'd0;

reg pulse;

wire tx;

wire can\_bitstuff;

wire txing;

wire out;

// Instantiate the modules

can\_tx dut (

.tx(tx),

.can\_bitstuff(can\_bitstuff),

.txing(txing),

.rx(rx),

.address(address),

.clk(clk),

.baud\_clk(baud\_clk),

.rst(rst),

.data(data),

.send\_data(send\_data),

.bitstuffed\_output(bitstuffed\_output),

.clear\_to\_tx(clear\_to\_tx)

);

OneShot os (

.pulse(pulse),

.clk(clk),

.rst(rst),

.out(out)

);

// Clock generation

always #((CLK\_PERIOD/2)) clk = ~clk;

always #5 baud\_clk = ~baud\_clk;

initial begin

rst = 1;

#20 rst = 0;

#50 send\_data = 1;

#10 send\_data = 0;

#100 rx = 1;

#10 rx = 0;

#50 address = 11'd123;

#70 data = 8'd255;

#150 pulse = 1;

#10 pulse = 0;

#200 $finish;

end

// Display output

always @(posedge clk) begin

$display("Time = %0t: tx = %b, can\_bitstuff = %b, txing = %b, out = %b", $time, tx, can\_bitstuff, txing, out);

end

initial begin

$dumpfile("dump.vcd");

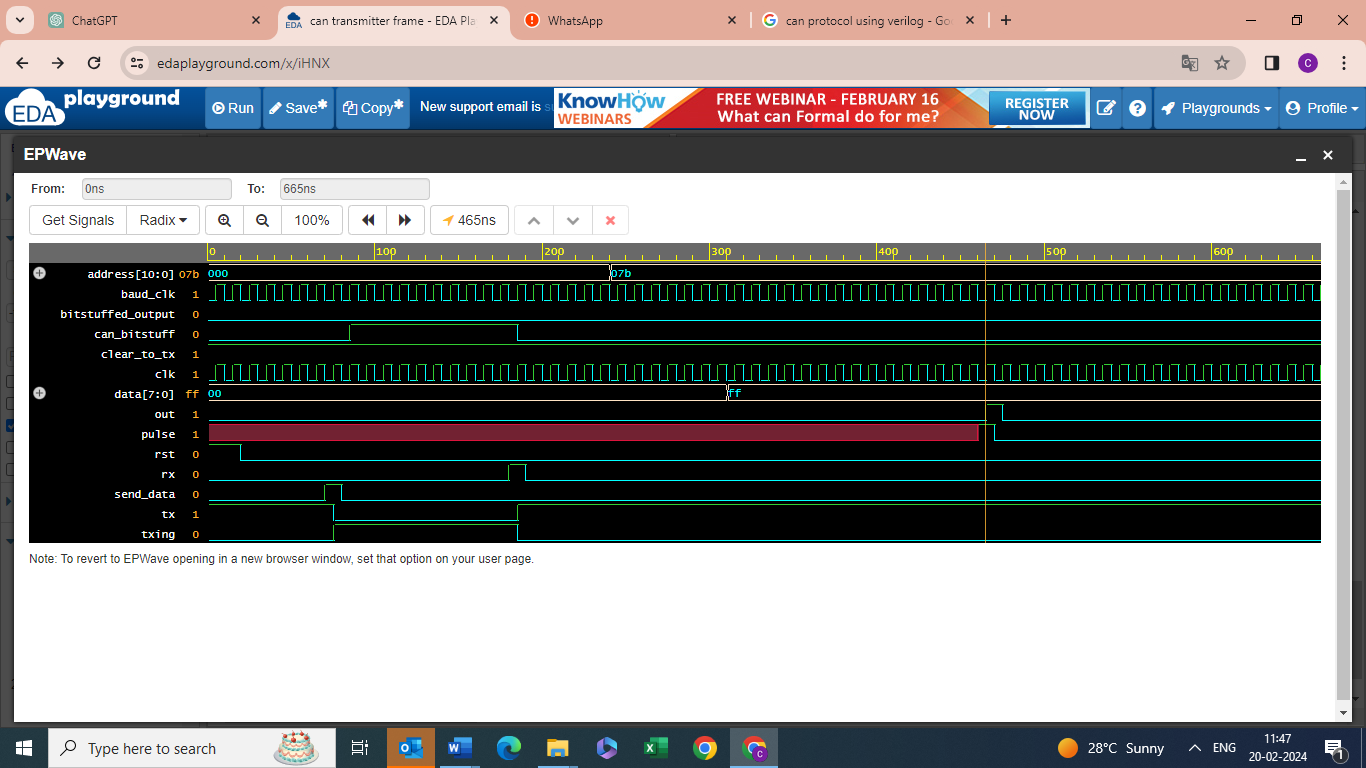
$dumpvars(0);

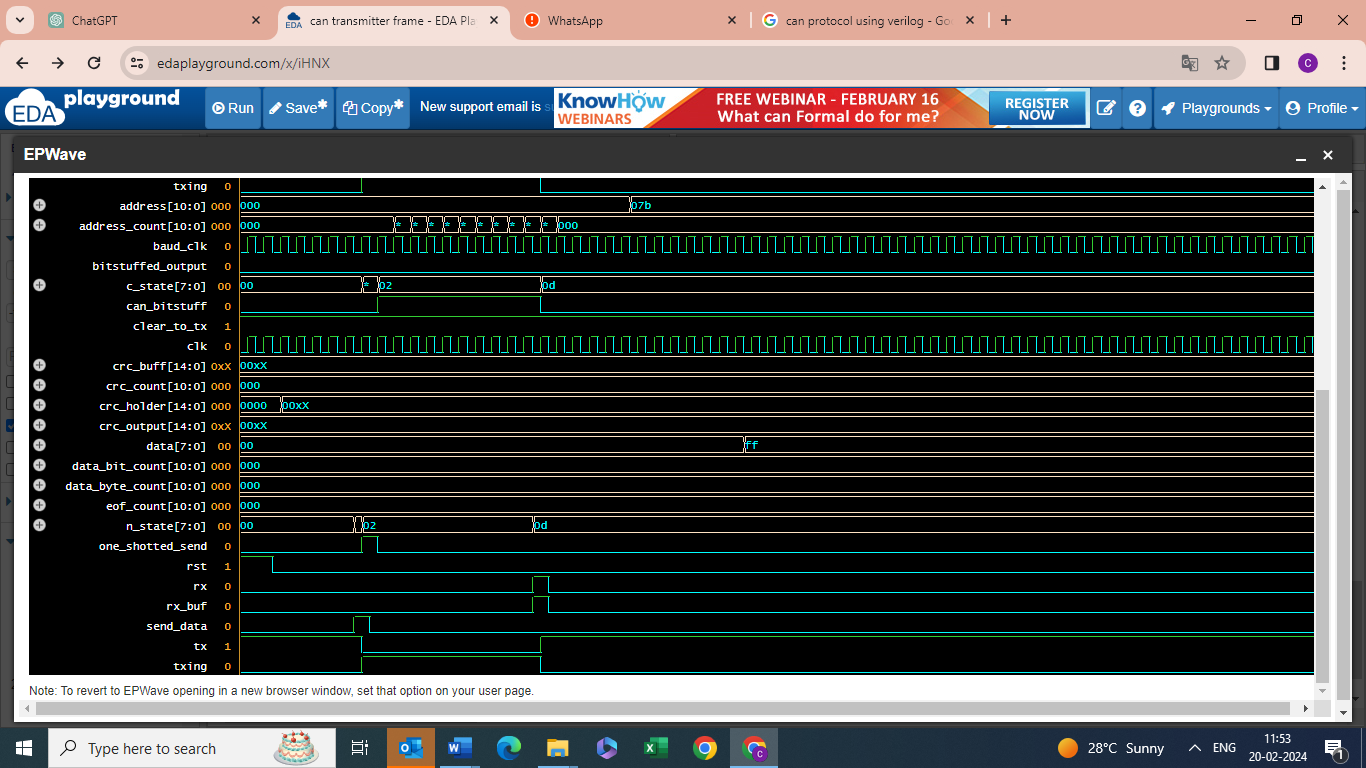
end

endmodule

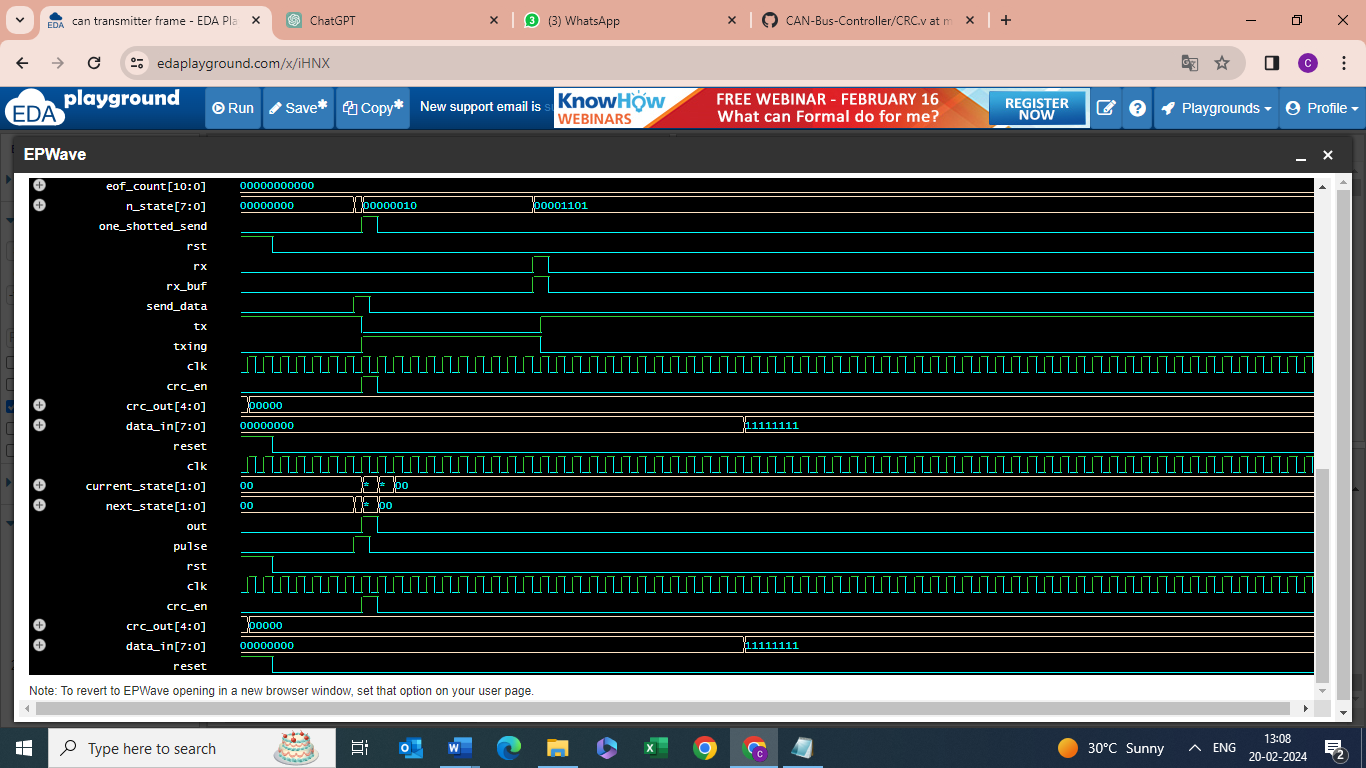
**OUTPUT:**

**Can\_tx\_tb**

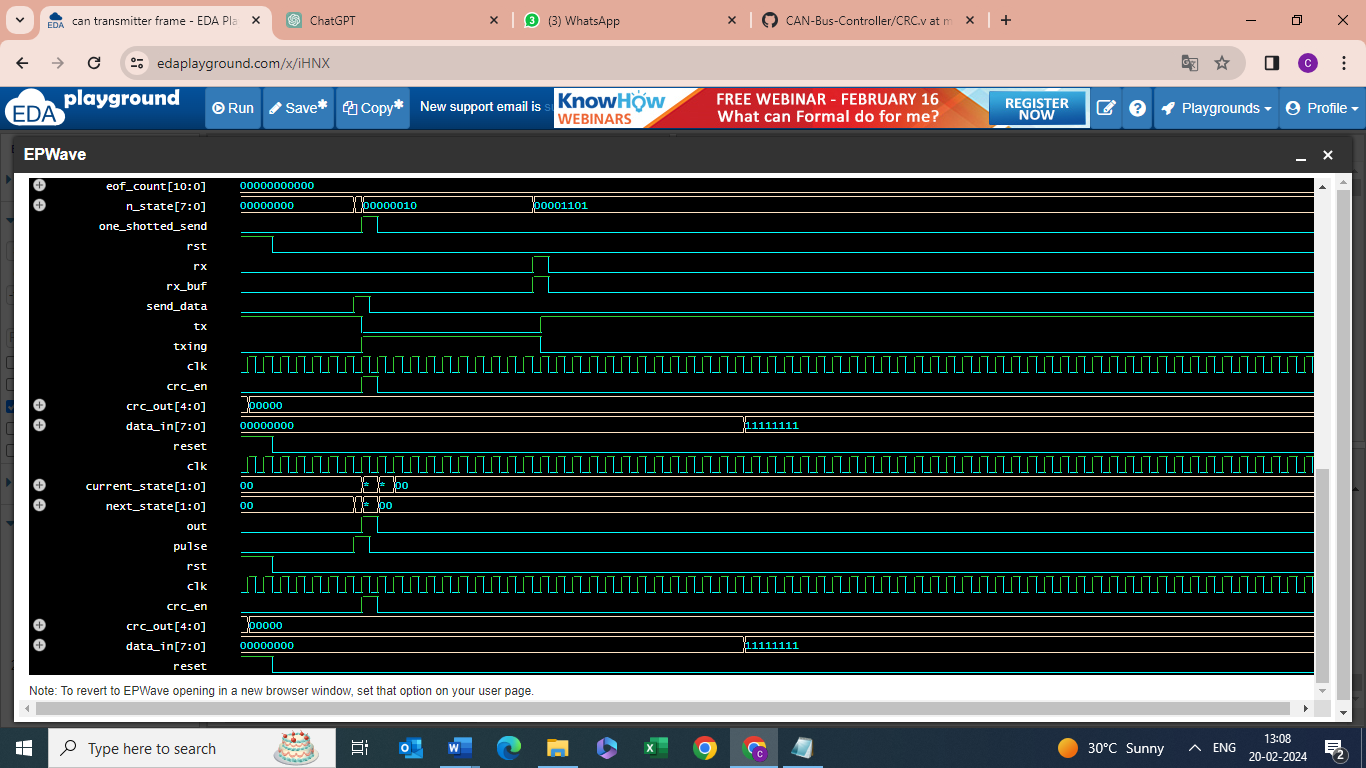


**Dut\_tb:**

**os\_tb:**



**crc\_tb:**



Time = 5: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 15: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 25: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 35: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 45: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 55: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 65: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 75: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 85: tx = 0, can\_bitstuff = 0, txing = 1, out = 0

Time = 95: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 105: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 115: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 125: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 135: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 145: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 155: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 165: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 175: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 185: tx = 0, can\_bitstuff = 1, txing = 1, out = 0

Time = 195: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 205: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 215: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 225: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 235: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 245: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 255: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 265: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 275: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 285: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 295: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 305: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 315: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 325: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 335: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 345: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 355: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 365: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 375: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 385: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 395: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 405: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 415: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 425: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 435: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 445: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 455: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 465: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 475: tx = 1, can\_bitstuff = 0, txing = 0, out = 1

Time = 485: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 495: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 505: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 515: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 525: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 535: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 545: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 555: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 565: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 575: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 585: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 595: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 605: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 615: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 625: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 635: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 645: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 655: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

Time = 665: tx = 1, can\_bitstuff = 0, txing = 0, out = 0

$finish called from file "testbench.sv", line 68.